REMARKS/ARGUMENTS

Claims 1-20 were pending. Upon entry of this amendment, claims 1, 15, 17, and 18 are amended, leaving claims 1-20 pending examination. Claims 1-20 stand rejected under 35 USC § 102 as being anticipated by U.S. Patent No. 5,847,580 issued to Bapat et al. (hereafter "Bapat"). Applicants aver that no new matter has been added in this response.

§102 Rejections

Claims 1, 15, 17, 18

In the Office Action, the Examiner rejected claims 1-20 under 35 USC § 102(b) as being anticipated by Bapat. For at least the reasons stated below, the Applicants respectfully request reconsideration and withdrawal of the rejections, as each of the claims as amended are patentable over Bapat.

With regard to claims 1, 15, 17, and 18, in the Office Action the Examiner stated that Bapat includes a PLD having a plurality of logic elements and a routing structure having a plurality of OR gates (85a..85d, Fig. 14) where each OR gate has at least one input connected to a respective one of the logic elements, where each OR gate, except and end OR gate having an output connected to a second input of a respective succeeding one of said OR gates. The Examiner states that a signal appearing on one of the OR gates appears on the final OR gate in the line, where the signal appearing on the final OR gate may be passed to a second group of logic elements. The Applicants respectfully submit that this assertion does not adequately show that all of claim limitations are taught or suggested in Bapat.

The Applicants submit that Bapat fails to disclose all the elements of claims 1, 15, 17, and 18. For example, amended claims 1 and 15 recite in part "a return line, comprising a plurality of drivers connected in series, each of said drivers having a connection to a respective one of a plurality of said logic elements in a second group of logic elements", amended claim 17 recites in part, the "routing structure is distinct from a programmable interconnect structure of the programmable logic device", and amended claim 18 recites in part, the "outputs from said first plurality of logic elements are multiplexed together, and made available to said second

plurality of logic elements via a return line coupled to an end OR gate of the plurality of distributed OR gates".

Bapat discloses multiplexer chains, each having an output coupled to an input of two logic gates. The two logic gates are used to output signals from the multiplexer chain in different directions to provide bi-directional signal distribution. Bapat discloses the output signal of a multiplexer chain divided into a top OR chain and a bottom OR chain. The top OR chain combines all the output of the multiplexer chains to its left, and the bottom OR chain combines all of the multiplexer chains to its right. The top OR chain and bottom OR chains propagate their respective output signals in different directions. The top OR chain and bottom OR chain are connected via respective multiplexers, e.g., the output of each OR gate is coupled to a multiplexer input and an output of the multiplexer is coupled to an input of another OR gate. Signals transmitted from an end logic OR chain rely on the programmable interconnect structure of the PLD to couple one logic unit to another logic unit (Bapat, Figs. 4-5, 7, 8, 10, 12-18, col. 3, line 60 to column 4 line 4, col. 4, lines 44-48, col. 6, lines 47-52).

There is nothing in Bapat that discloses or suggests a return line comprising a plurality of drivers connected in series, as recited in amended claim 1 and 15, nor a routing structure distinct from the programmable interconnect structure of the programmable logic device as recited in amended claim 17, nor where outputs from a first plurality of logic elements are multiplexed together and made available to a second plurality of logic elements via a return line coupled to an end OR gate of the plurality of distributed OR gates as recited in amended claim 18. Claims 1, 15, 17, and 18 are thus patentably distinguished over Bapat for at least the above reasons.

Dependent Claims 2-14, 16, and 19-20

Claims 2-14 depend from amended claim 1, claim 16 depends from amended claim 15, and claims 19-20 depend from amended claim 18 and are therefore patentable for at least the above reasons. These claims, however recite additional elements that further distinguish over the cited art. For example, claim 2 recites in part "the first group of logic elements and the second group of logic elements are mutually exclusive", claim 3 recites in part

"the first group of logic elements and the second group of logic elements contain at least one logic element in common", and claims 4-14 recite in part "the logic elements in said programmable logic device are arranged in an array, the array comprising rows and columns of logic elements." Claim 16 recites in part the "routing lines of said first plurality of routing lines and of said second plurality of routing lines are connected to respective logic elements spaced apart along said rows of logic elements", claim 19 partially recites "outputs from said second plurality of logic elements are multiplexed together, and made available to said first plurality of logic elements' and claim 20 partially recites "allocating functionality to said first plurality of logic elements such that they form parts of respective bus master devices, and allocating functionality to said second plurality of logic elements such that they form parts of respective slave devices in said bus structure". Dependent claims 2-14, 16, and 19-20 are therefore patentably distinguished over Bapat. Accordingly, withdrawal of the rejection of claims 2-14, 16, and 19-20 is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

C. Bart Sullivan
Reg. No. 41,516

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
CBS:rgy

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